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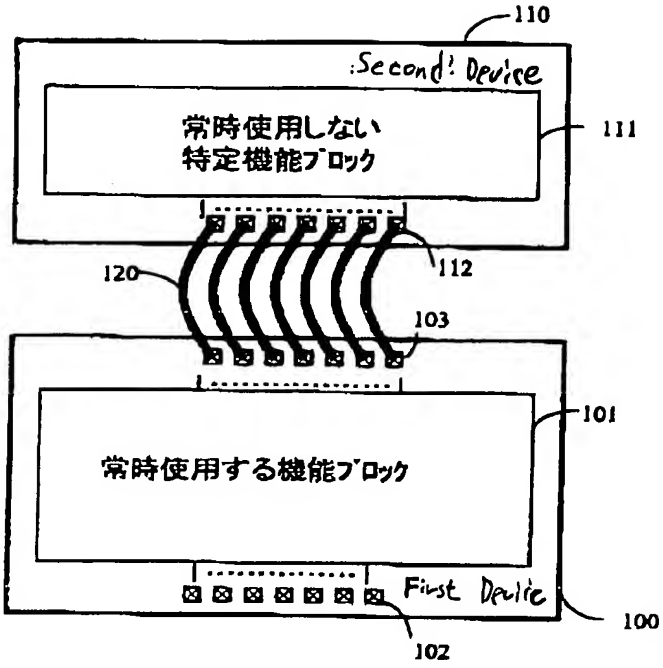
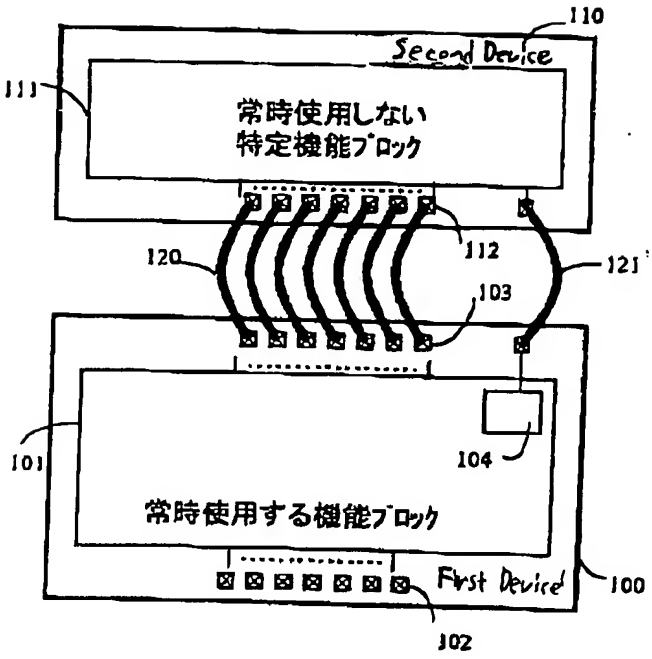
Fig.1



100 常時使用しない特定機能ブロックを除いた半導体装置(第1の装置)
101 常時使用する機能ブロック
102 第1の装置の制御端子
103 制御バス端子
110 常時使用しない特定機能装置(第2の装置)
111 常時使用しない特定機能ブロック
112 制御バス端子
120 接続線

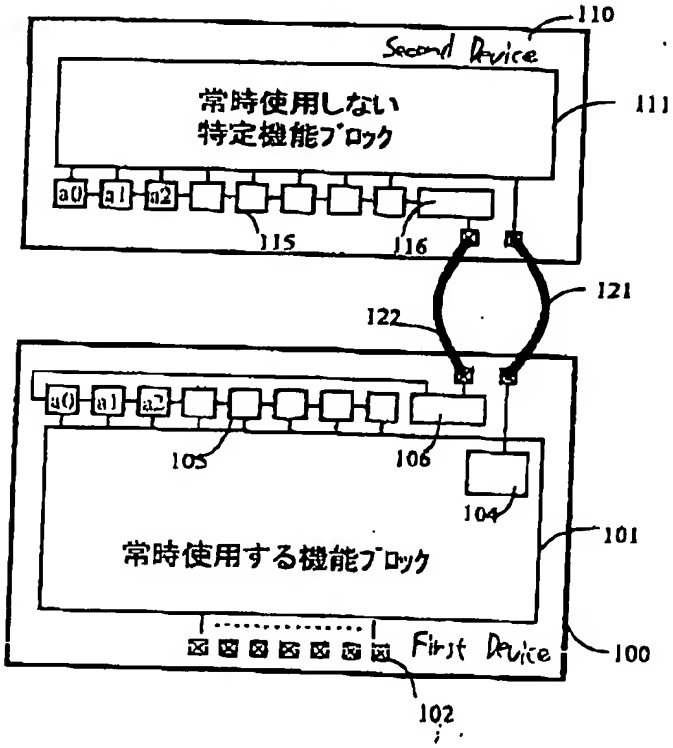
100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
103: CONTROL BUS TERMINAL
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
112: CONTROL BUS TERMINAL
120: CONNECTION LINE

Fig.2



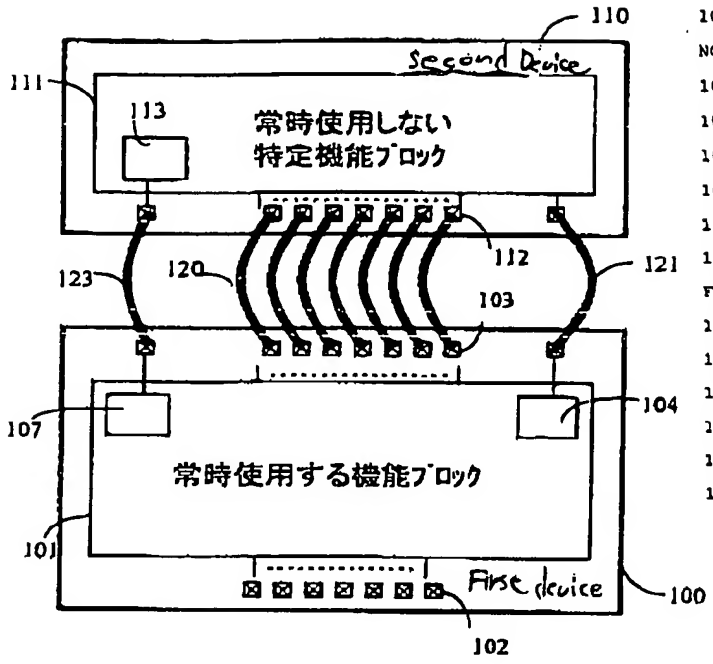
100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
103: CONTROL BUS TERMINAL
104: SECOND DEVICE CONTROL START SIGNAL GENERATION CIR.
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FURCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
112: CONTROL BUS TERMINAL
120: CONNECTION LINE
121: SECOND DEVICE CONTROL START SIGNAL LINE

Fig.3



100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
104: SECOND DEVICE CONTROL START SIGNAL GENERATION CIR.
105: CONTROL SIGNAL REGISTER GROUP OF FIRST DEVICE
106: SERIAL I/F OF FIRST DEVICE
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
115: CONTROL SIGNAL REGISTER GROUP OF SECOND DEVICE
116: SERIAL I/F OF SECOND DEVICE
121: SECOND DEVICE CONTROL START SIGNAL LINE
122: SERIAL CONTROL SIGNAL LINE

Fig. 4



100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK

101: ALWAYS-USED FUNCTION BLOCK

102: CONTROL TERMINAL OF FIRST DEVICE

103: CONTROL BUS TERMINAL

104: SECOND DEVICE CONTROL START SIGNAL GENERATION CIR.

107: SECOND DEVICE DETECTION CIR.

110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION

111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK

112: CONTROL BUS TERMINAL

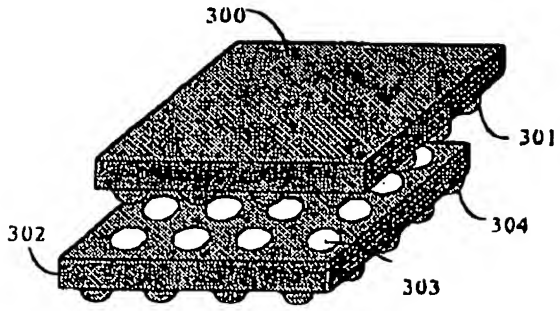
113: IDENTIFICATION SIGNAL GENERATION CIR.

120: CONNECTION LINE

121: SECOND DEVICE CONTROL START SIGNAL LINE

123: SECOND DEVICE IDENTIFICATION SIGNAL LINE

Fig. 5



300: PACKAGE INCORPORATING SECOND DEVICE

301: BALL GRID ARRAY ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

302: PACKAGE INCORPORATING FIRST DEVICE

303: PACKAGE CONTACT SURFACES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL BUS TERMINALS OF FIRST DEVICE)

304: BALL GRID ARRAY ELECTRODES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL TERMINALS OF FIRST DEVICE)

Fig. 6

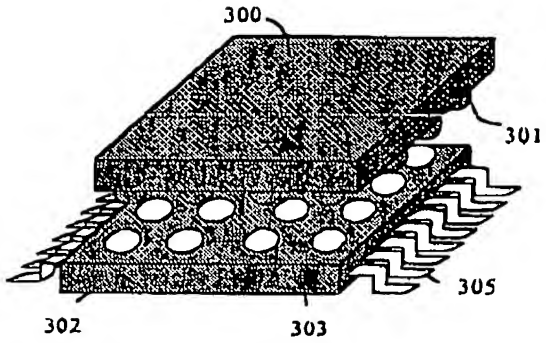
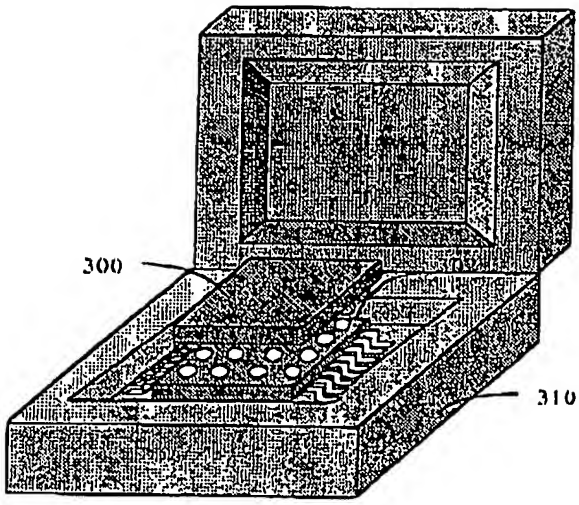


Fig. 7

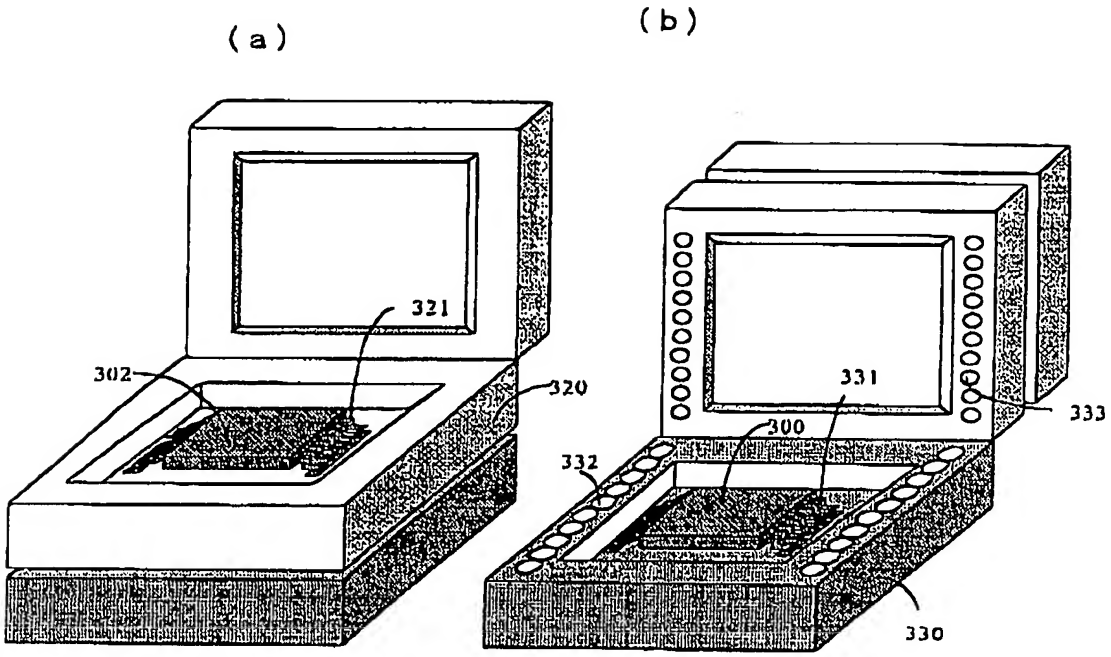


300: PACKAGE INCORPORATING SECOND DEVICE

302: PACKAGE INCORPORATING FIRST DEVICE

310: SOCKET FOR CONNECTING TWO PACKAGES

Fig. 8



300: PACKAGE INCORPORATING SECOND DEVICE

302: PACKAGE INCORPORATING FIRST DEVICE

320: FIRST PACKAGE INSERTION PORTION OF 2-STAGE CONNECTION SOCKET

321: ELECTRODES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

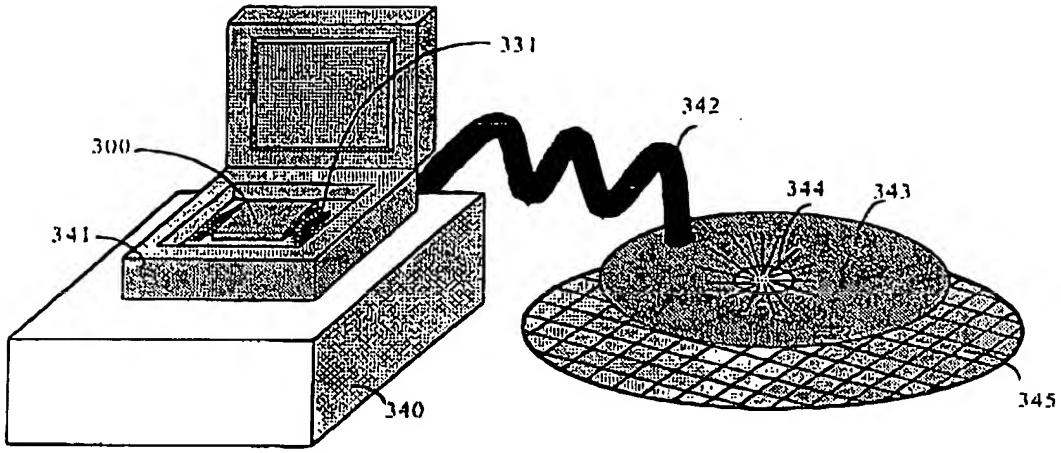
330: SECOND PACKAGE INSERTION PORTION OF 2-STAGE CONNECTION SOCKET

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

332: CONNECTION SIGNAL ELECTRODES CONNECTED TO SECOND PACKAGE (CONTROL BUS TERMINALS OF SECOND DEVICE)

333: CONNECTION SIGNAL ELECTRODES CONNECTED TO FIRST PACKAGE (CONTROL BUS TERMINALS OF SECOND DEVICE)

Fig.9



300: PACKAGE INCORPORATING SECOND DEVICE

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

340: APPARATUS (E.G., GENERAL-PURPOSE TESTING APPARATUS) FOR SETTING FUNCTION IN FIRST DEVICE

341: SOCKET IN WHICH SECOND PACKAGE IS INSERTED

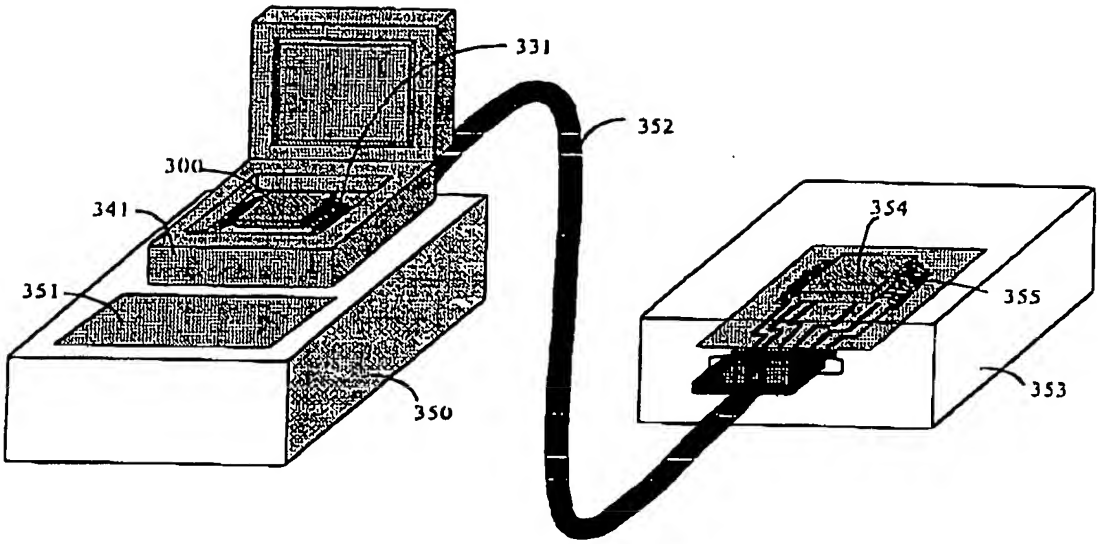
342: CONNECTION LINE (FOR CONTROL BUS TERMINALS SIGNALS FROM FIRST DEVICE AND CONTROL TERMINAL SIGNALS FROM SECOND DEVICE)

343: PROBE CARD

344: PROBE ELECTRODES (CONTROL BUS TERMINALS FOR FIRST DEVICE AND CONTROL TERMINALS FOR SECOND DEVICE)

345: WAFER ON WHICH FIRST DEVICES ARE FORMED

Fig. 10



300: PACKAGE INCORPORATING SECOND DEVICE

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

341: SOCKET IN WHICH SECOND PACKAGE IS INSERTED

350: APPARATUS (E.G., GENERAL-PURPOSE REWRITING APPARATUS) FOR SETTING FUNCTIONS IN FIRST DEVICE

351: MANIPULATION SURFACE OF FUNCTION SETTING APPARATUS

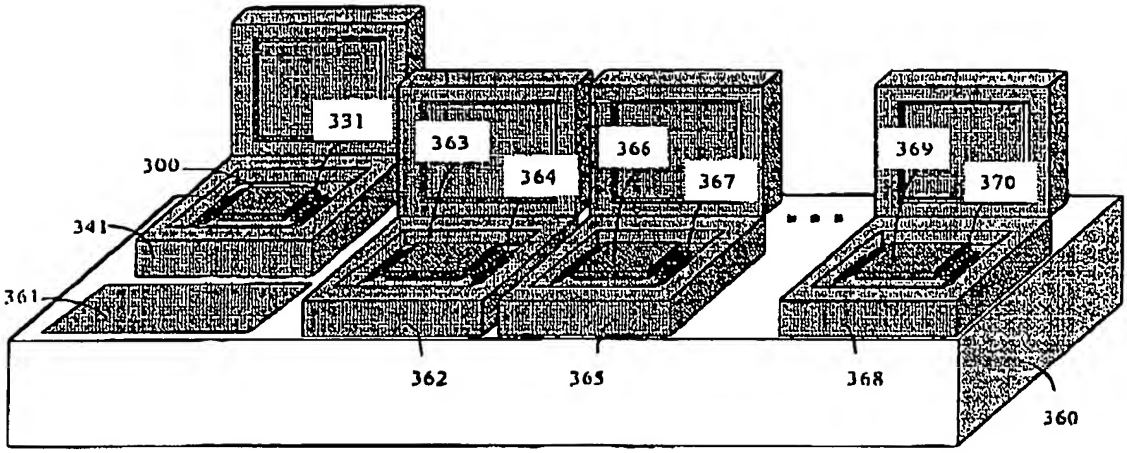
352: CONNECTION LINE (FOR CONTROL BUS TERMINALS SIGNALS FROM FIRST DEVICE AND CONTROL TERMINAL SIGNALS FROM SECOND DEVICE)

353: APPARATUS (E.G., CELLULAR PHONE) INCORPORATING FIRST DEVICE

354: PACKAGE INCORPORATING FIRST DEVICE

355: ELECTRODES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL BUS TERMINALS FOR FIRST DEVICE AND CONTROL TERMINALS FOR SECOND DEVICE)

Fig.11



300: PACKAGE INCORPORATING SECOND DEVICE

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

341: SOCKET IN WHICH SECOND PACKAGE IS INSERTED

360: APPARATUS (E.G., GENERAL-PURPOSE REWRITING APPARATUS) FOR SETTING FUNCTIONS IN FIRST DEVICE

361: MANIPULATION SURFACE OF FUNCTION SETTING APPARATUS

362: SOCKET IN WHICH FIRST FIRST PACKET IS INSERTED

363: PACKAGE INCORPORATING FIRST FIRST DEVICE

364: ELECTRODES OF PACKAGE INCORPORATING FIRST FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

365: SOCKET IN WHICH SECOND FIRST PACKET IS INSERTED

366: PACKAGE INCORPORATING SECOND FIRST DEVICE

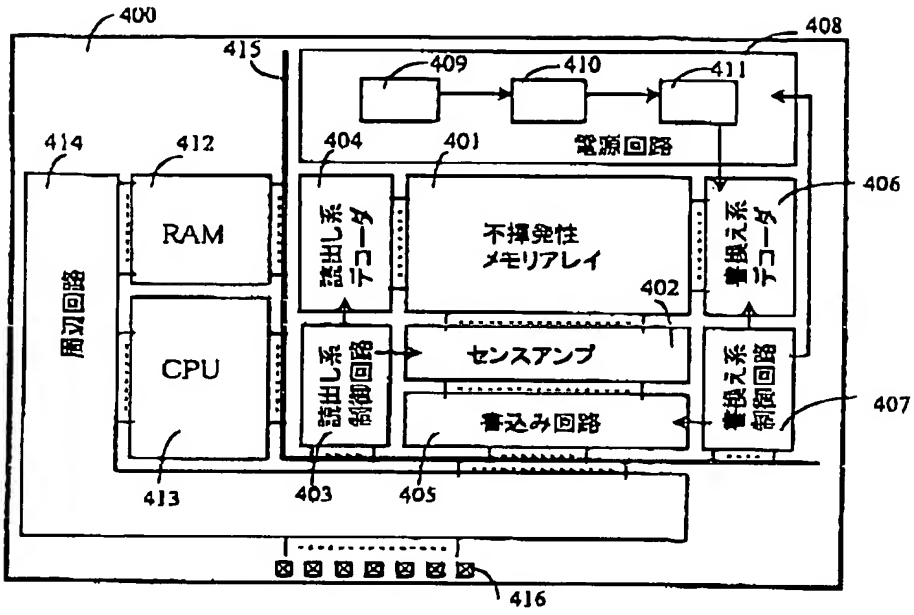
367: ELECTRODES OF PACKAGE INCORPORATING SECOND FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

368: SOCKET IN WHICH NTH FIRST PACKET IS INSERTED

366: PACKAGE INCORPORATING NTH FIRST DEVICE

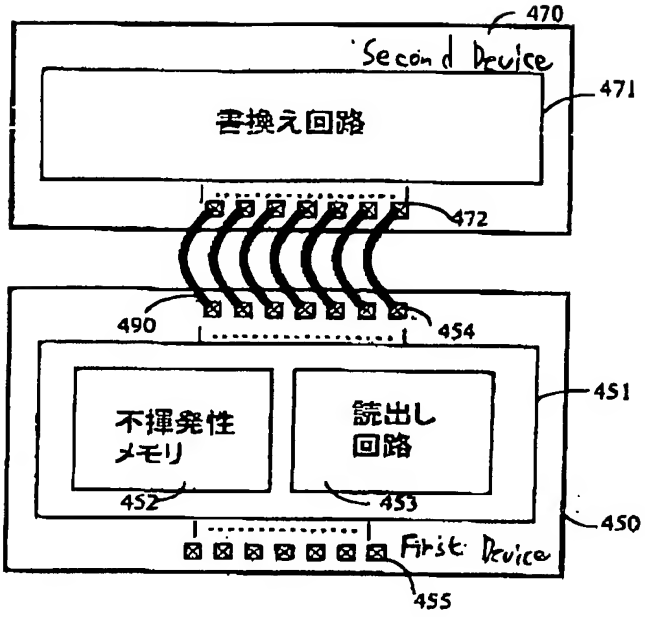
367: ELECTRODES OF PACKAGE INCORPORATING NTH FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

Fig.12



400: NONVOLATILE-MEMORY-INCORPORATED MICROCOMPUTER
401: NONVOLATILE MEMORY CELL ARRAY
402: SENSE AMPLIFIER CIR.
403: READING CONTROL CIR.
404: READING DECODER
405: WRITING CIR. (PAGE LATCH)
406: REWRITING DECODER
407: REWRITING CONTROL CIR.
408: POWER CIR.
409: REFERENCE VOLTAGE TRIMMING CIR.
410: REFERENCE VOLTAGE GENERATION CIR.
411: REWRITING VOLTAGE GENERATION CIR.
414: PERIPHERAL CIRCUITS
415: CONTROL BUS
416: MICROCOMPUTER CONTROL TERMINAL

Fig.13



450: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK

451: READ-ONLY NONVOLATILE MEMORY BLOCK

452: NONVOLATILE MEMORY

453: READING CIR.

454: REWRITING CONTROL BUS TERMINAL

455: CONTROL TERMINAL OF FIRST DEVICE

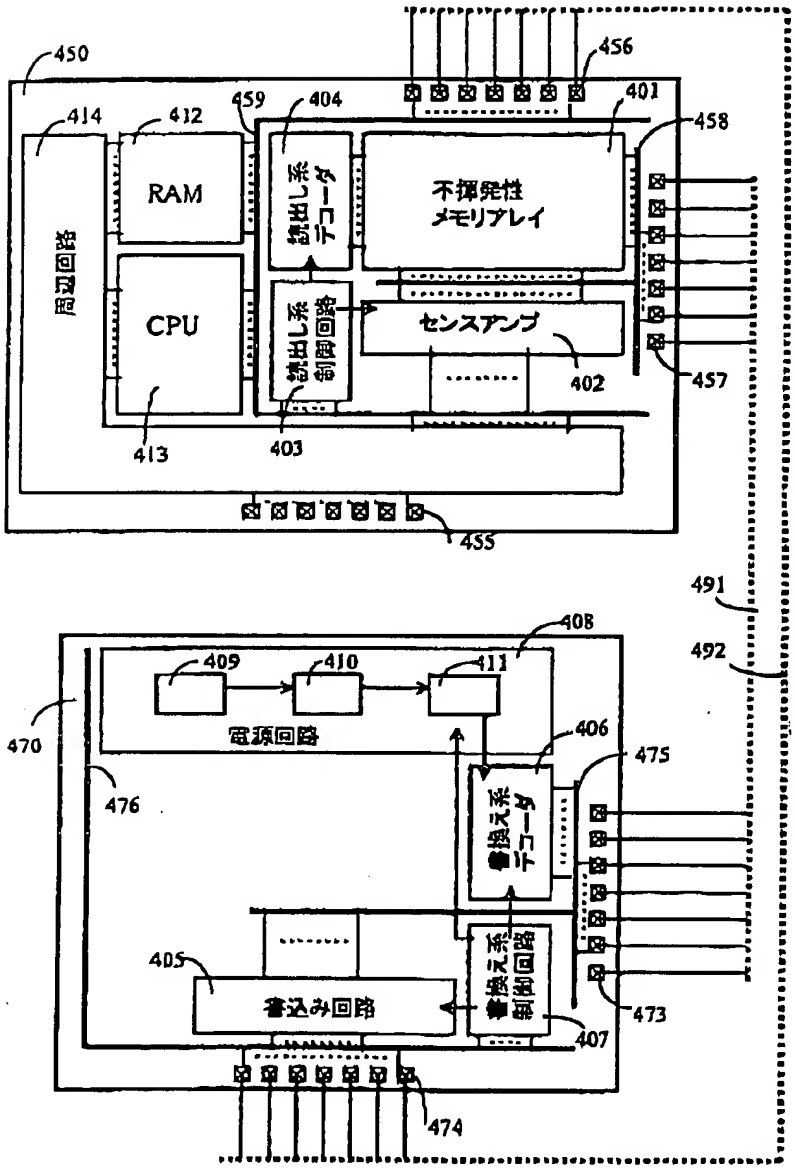
470: FIRST DEVICE REWRITING DEVICE (SECOND DEVICE)

471: FIRST DEVICE REWRITING CIR.

472: REWRITING CONTROL BUS TERMINAL

490: REWRITING SIGNAL LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

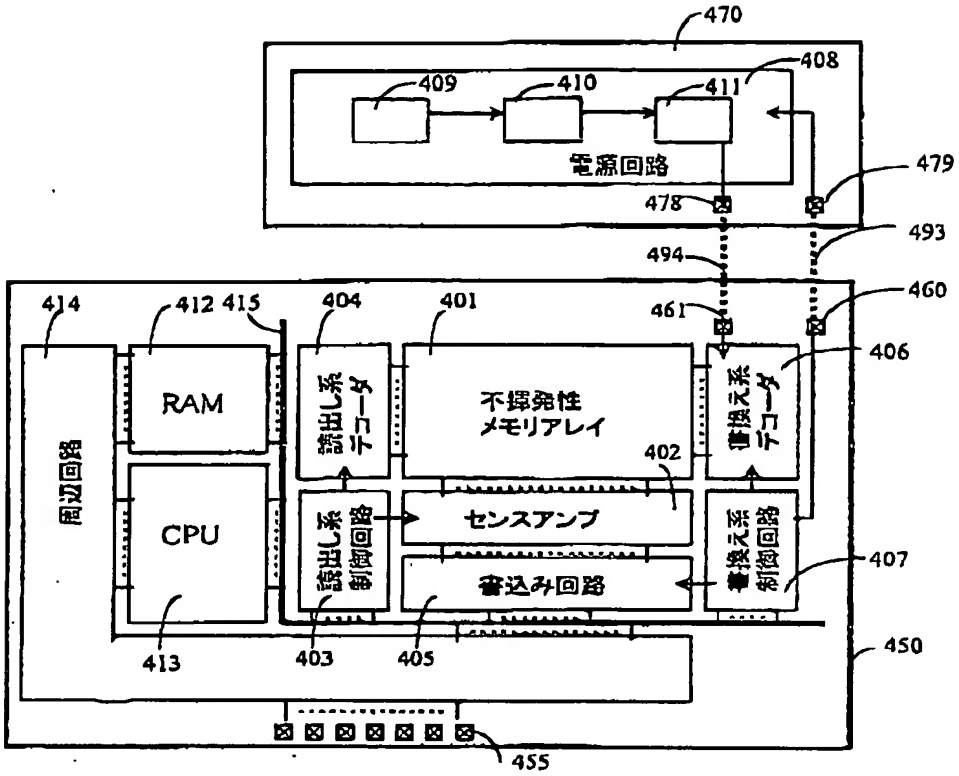
Fig. 14



401: NONVOLATILE MEMORY CELL ARRAY
402: SENSE AMPLIFIER CIR.
403: READING CONTROL CIR.
404: READING DECODER
405: WRITING CIR. (PAGE LATCH)
406: REWRITING DECODER
407: REWRITING CONTROL CIR.
408: POWER CIR.
409: REFERENCE VOLTAGE TRIMMING CIR.
410: REFERENCE VOLTAGE GENERATION CIR.
411: REWRITING VOLTAGE GENERATION CIR.
414: PERIPHERAL CIRCUITS
450: MICROCOMPUTER INCORPORATING READ-ONLY NONVOLATILE MEMORY (FIRST DEVICE)
455: CONTROL TERMINAL OF FIRST DEVICE
456: REWRITING CONTROL CONNECTION TERMINAL GROUP
457: REWRITING SIGNAL CONNECTION TERMINAL GROUP
458: REWRITING CONTROL BUS
459: CONTROL BUS
470: DEVICE (SECOND DEVICE) FOR REWRITING NONVOLATILE MEMORY OF FIRST DEVICE
473: REWRITING SIGNAL CONNECTION TERMINAL GROUP
474: REWRITING CONTROL CONNECTION TERMINAL GROUP
475: REWRITING CONTROL BUS
476: CONTROL BUS

491: REWRITING BUS SIGNAL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)
492: BUS CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

Fig.15



401: NONVOLATILE MEMORY CELL ARRAY

402: SENSE AMPLIFIER CIR.

403: READING CONTROL CIR.

404: READING DECODER

405: WRITING CIR. (PAGE LATCH)

406: REWRITING DECODER

407: REWRITING CONTROL CIR.

408: POWER CIR.

409: REFERENCE VOLTAGE TRIMMING CIR.

410: REFERENCE VOLTAGE GENERATION CIR.

411: REWRITING VOLTAGE GENERATION CIR.

414: PERIPHERAL CIRCUITS

415: CONTROL BUS

450: MICROCOMPUTER INCORPORATING READ-ONLY NONVOLATILE MEMORY (FIRST DEVICE)

455: CONTROL TERMINAL OF FIRST DEVICE

460: REWRITING CONTROL TERMINAL

461: REWRITING POWER CONNECTION TERMINAL

470: POWER DEVICE (SECOND DEVICE) FOR REWRITING NONVOLATILE MEMORY OF FIRST DEVICE

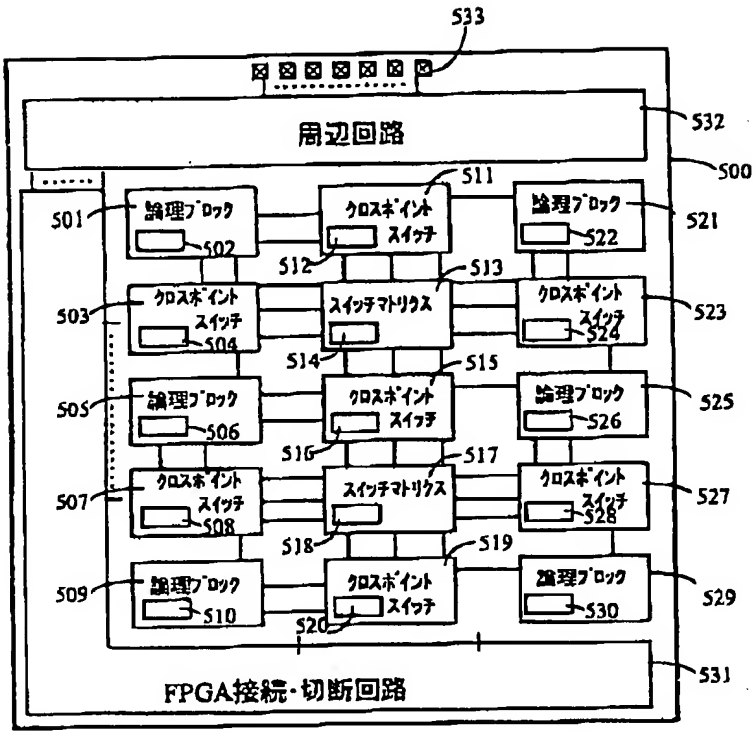
478: REWRITING POWER CONNECTION TERMINAL

479: REWRITING CONTROL TERMINAL

493: REWRITING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

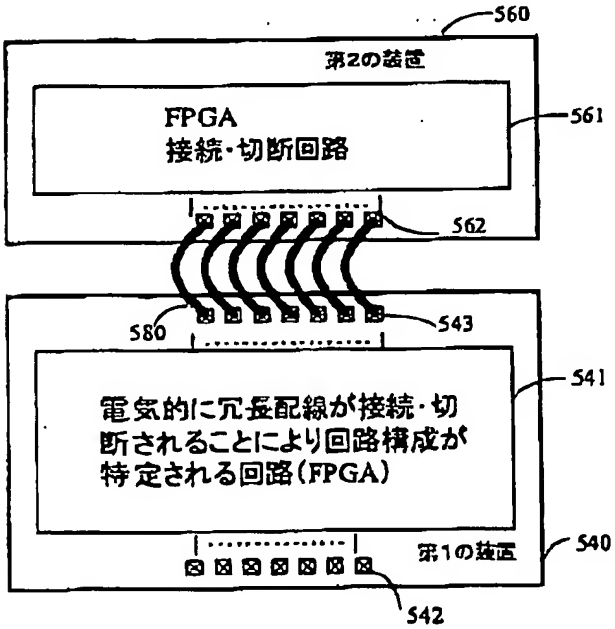
494: REWRITING POWER CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

Fig.16



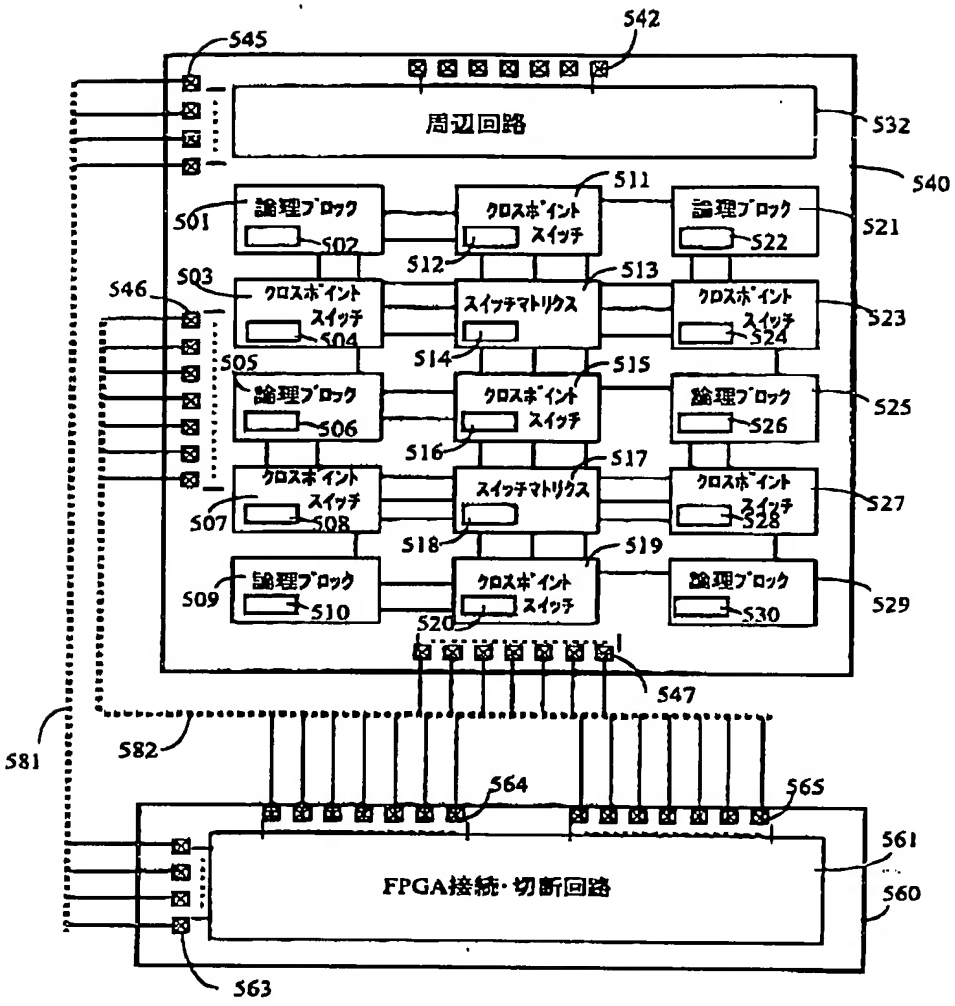
500 FPGA
(Field Programmable Gate Array)
501,505,509,521,525,529 LOGIC BLOCK
502,506,510,522,526,530 LOGIC BLOCK SETTING MEMORY
503,507,511,515,519,523,527 CROSS POINT SWITCH
504,508,512,516,520,524,528 CROSS POINT SWITCH SETTING MEMORY
513, 517: SWITCH MATRIX
514, 518: SWITCH MATRIX SETTING MEMORY
531: FPGA CONNECTING/DISCONNECTING CIR.
532: PERIPHERAL CIRCUITS
533: FPGA CONTROL TERMINAL

Fig.17



540: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY CONNECTING AND DISCONNECTING REDUNDANT WIRING ELECTRICALLY
541: CIRCUIT (FPGA) WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY CONNECTING AND DISCONNECTING REDUNDANT WIRING ELECTRICALLY
542: CONTROL TERMINAL OF FIRST DEVICE
543: CONNECTION/DISCONNECTION CONTROL TERMINAL
560: FIRST DEVICE CONNECTING/DISCONNECTING DEVICE (SECOND DEVICE)
561: FIRST DEVICE CONNECTING/DISCONNECTING CIR.
562: CONNECTION/DISCONNECTION CONTROL TERMINAL
580: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig. 18



501, 505, 509, 521, 525, 529: LOGIC BLOCK

502, 506, 510, 522, 526, 530: LOGIC BLOCK SETTING MEMORY

503, 509, 511, 515, 519, 523, 527: CROSS POINT SWITCH

504, 508, 512, 516, 520, 524, 528: CROSS POINT SWITCH SETTING MEMORY

513, 517: SWITCH MATRIX

514, 518: SWITCH MATRIX SETTING MEMORY

532: PERIPHERAL CIRCUITS

540: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY CONNECTING AND DISCONNECTING REDUNDANT WIRING ELECTRICALLY

542: CONTROL TERMINAL OF FIRST DEVICE

545: CONNECTION/DISCONNECTION CONTROL TERMINAL

546, 547: CONNECTION/DISCONNECTION SIGNAL TERMINAL

560: FIRST DEVICE (FPGA) CONNECTING/DISCONNECTING DEVICE (SECOND DEVICE)

561: FIRST DEVICE CONNECTING/DISCONNECTING CIR.

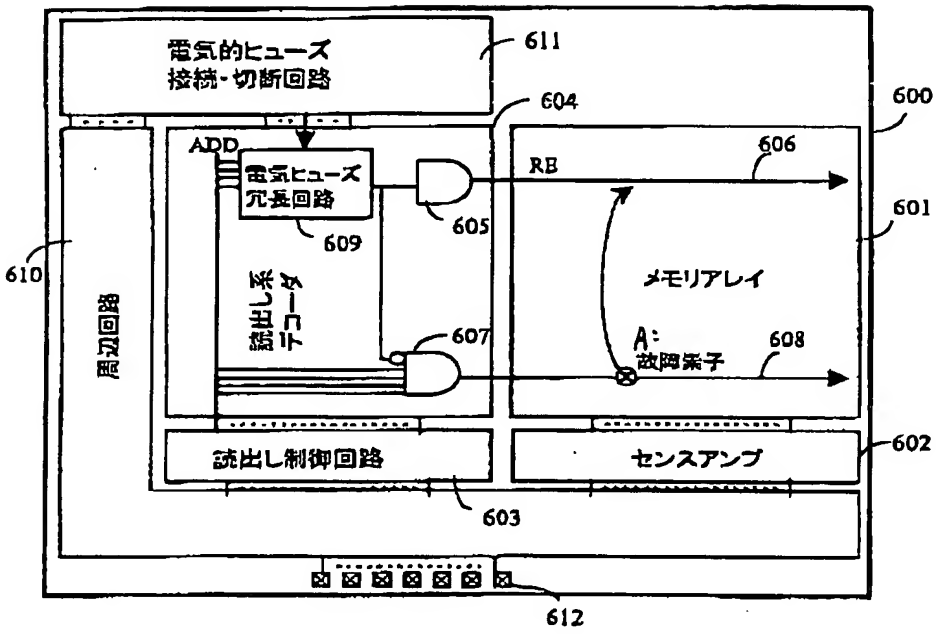
563: CONNECTION/DISCONNECTION CONTROL TERMINAL

564, 565: CONNECTION/DISCONNECTION SIGNAL TERMINAL

581: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

582: CONNECTION/DISCONNECTION SIGNAL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig.19



A: FAULTY ELEMENT

600: CIRCUIT WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES

601: MEMORY ARRAY

602: SENSE AMPLIFIER CIR.

603: READING CONTROL CIR.

604: READING DECODER

605: REDUNDANT DECODER

606: REDUNDANT WORD LINE

607: DECODER

608: WORD LINE

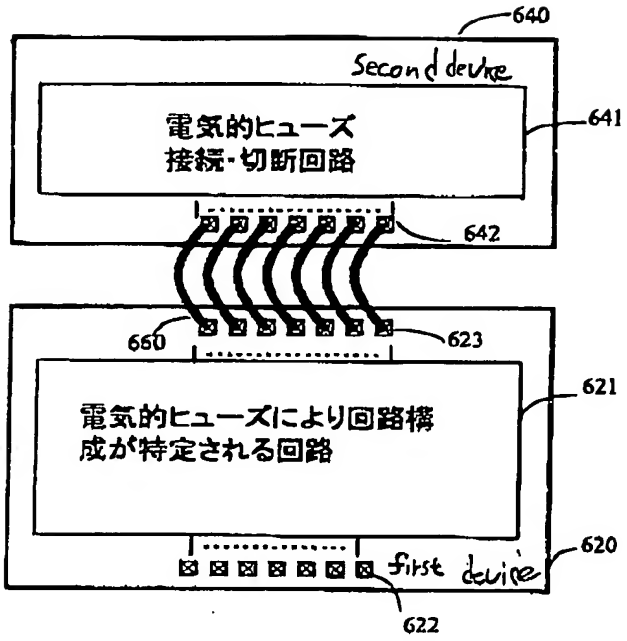
609: ELECTRIC FUSE REDUNDANT CIR.

610: PERIPHERAL CIRCUITS

611: ELECTRIC FUSE CONNECTING/DISCONNECTING CIR.

612: CONTROL TERMINAL OF SEMICONDUCTOR DEVICE

Fig.20



620: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES

621: CIRCUIT WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES

622: CONTROL TERMINAL OF FIRST DEVICE

623: CONNECTION/DISCONNECTION CONTROL TERMINAL

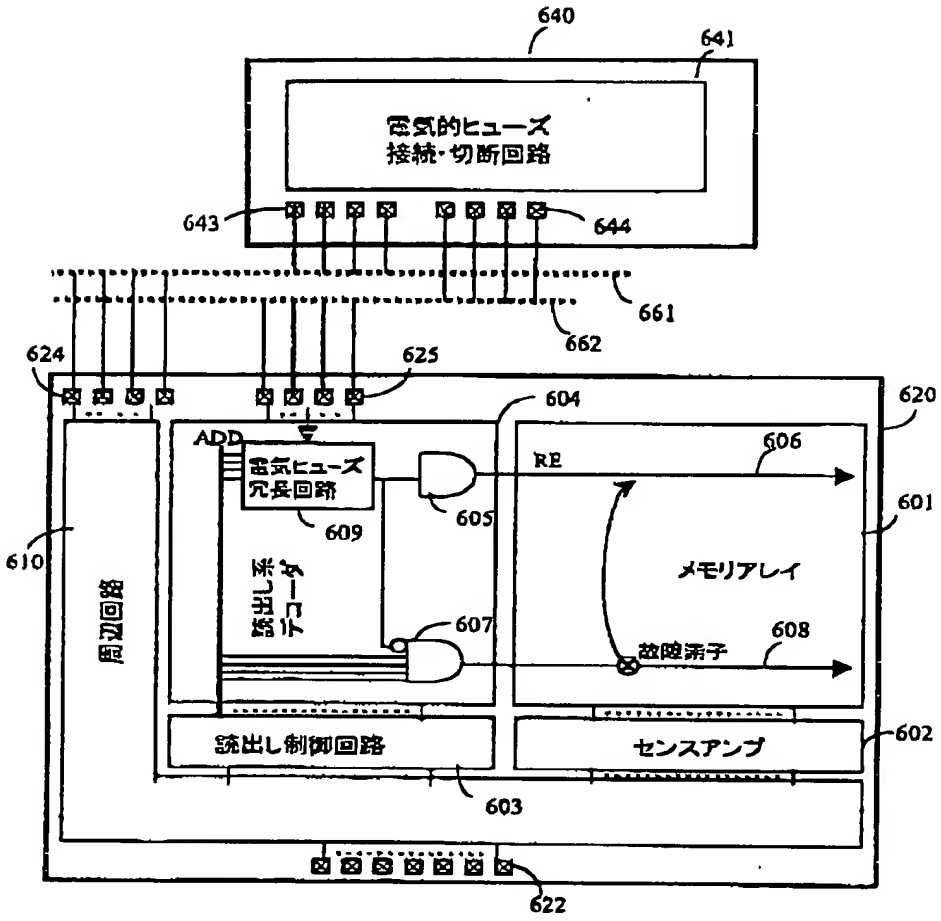
640: FIRST DEVICE CONNECTING/DISCONNECTING DEVICE (SECOND DEVICE)

641: FIRST DEVICE CONNECTING/DISCONNECTING CIR.

642: CONNECTION/DISCONNECTION CONTROL TERMINAL

660: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig.21



A: FAULTY ELEMENT

601: MEMORY ARRAY

602: SENSE AMPLIFIER CIR.

603: READING CONTROL CIR.

604: READING DECODER

605: REDUNDANT DECODER

606: REDUNDANT WORD LINE

607: DECODER

608: WORD LINE

609: ELECTRIC FUSE REDUNDANT CIR.

610: PERIPHERAL CIRCUITS

620: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES

622: CONTROL TERMINAL OF FIRST DEVICE

624: CONNECTION/DISCONNECTION CONTROL TERMINAL

625: CONNECTION/DISCONNECTION SIGNAL TERMINAL

640: DEVICE (SECOND DEVICE) FOR CONNECTING AND DISCONNECTING ELECTRIC FUSES OF FIRST DEVICE

641: DEVICE FOR CONNECTING AND DISCONNECTING ELECTRIC FUSES OF FIRST DEVICE

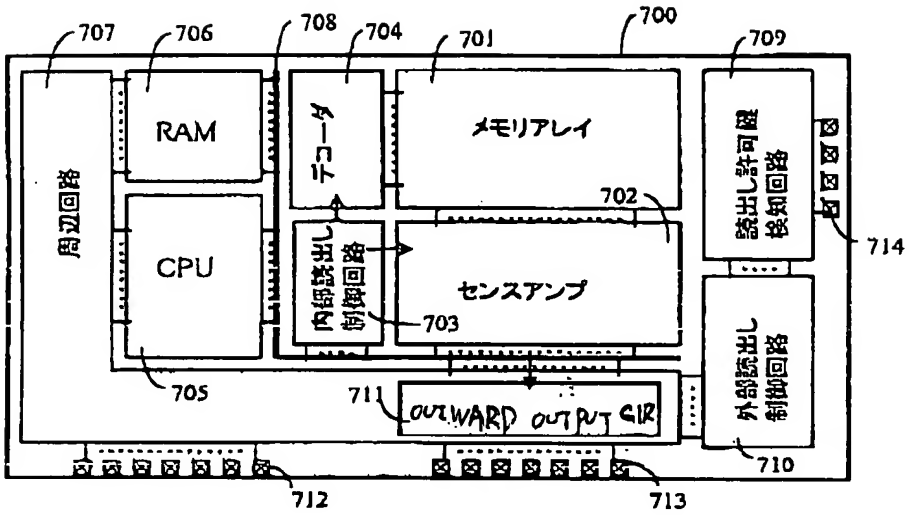
643: CONNECTION/DISCONNECTION CONTROL TERMINAL

644: CONNECTION/DISCONNECTION SIGNAL TERMINAL

661: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

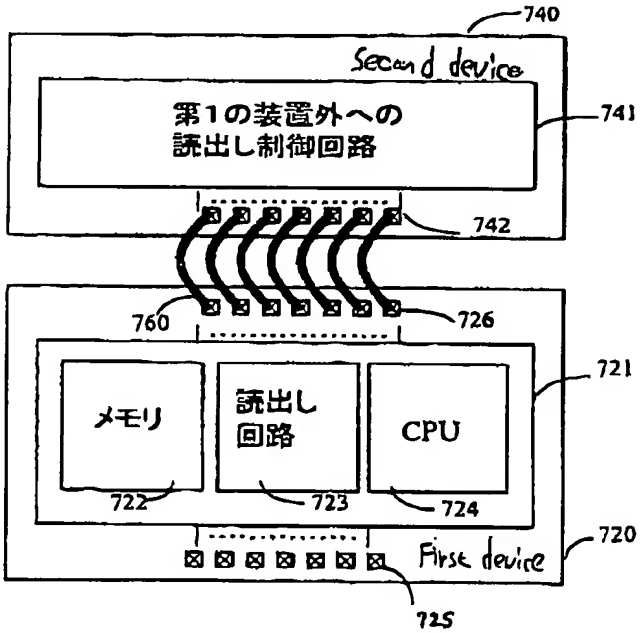
662: CONNECTION/DISCONNECTION SIGNAL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig.22



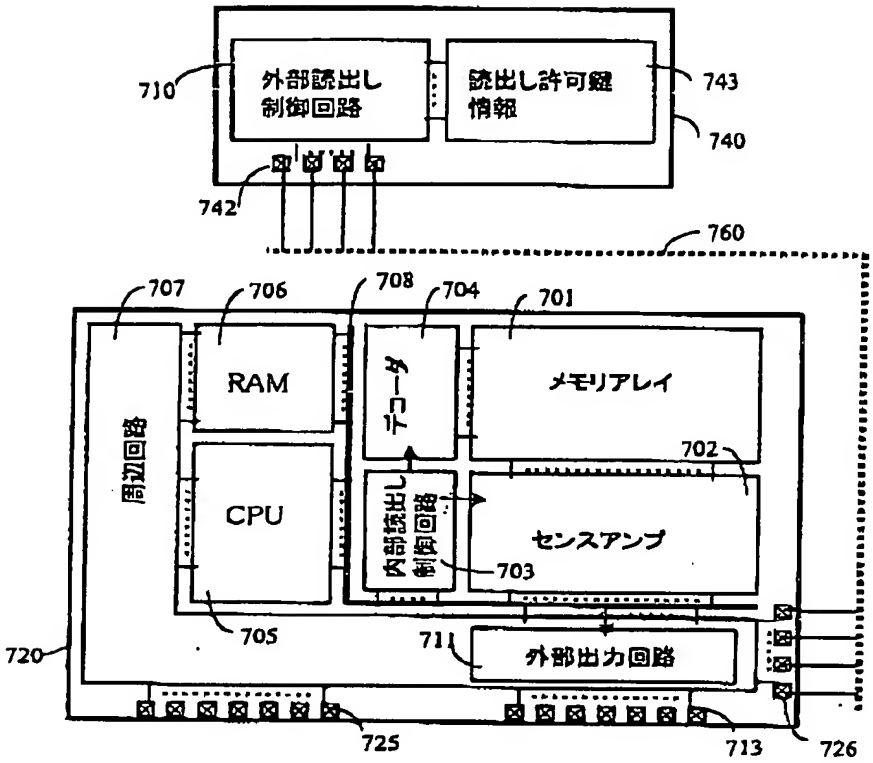
700: MICROCOMPUTER
701: MEMORY ARRAY
702: SENSE AMPLIFIER CIR.
703: MICROCOMPUTER INTERNAL READING CONTROL CIR.
704: READING DECODER
707: PERIPHERAL CIRCUITS
708: CONTROL BUS
709: READING PERMISSION KEY DETECTION CIR.
710: OUTWARD READING CONTROL CIR.
711: OUT-OF-MICROCOMPUTER OUTPUT CIR.
712: MICROCOMPUTER CONTROL TERMINAL
713: MEMORY DATA OUTPUT TERMINAL
714: READING PERMISSION KEY INPUT TERMINAL

Fig.23



720: MICROCOMPUTER (FIRST DEVICE) NOT HAVING OUT-OF-CHIP MEMORY DATA READING FUNCTION
721: CIRCUIT CAPABLE OF READING MEMORY DATA ONLY INSIDE CHIP
722: MEMORY
723: MICROCOMPUTER INTERNAL READING CIR.
725: CONTROL TERMINAL OF FIRST DEVICE
726: OUTWARD READING CONTROL TERMINAL
740: OUT-OF-FIRST-DEVICE READING CONTROL DEVICE (SECOND DEVICE)
741: OUT-OF-FIRST-DEVICE READING CONTROL CIR.
742: OUTWARD READING CONTROL TERMINAL
760: OUTWARD READING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF OUT-OF-CHIP READING)

Fig.29



701: MEMORY ARRAY

702: SENSE AMPLIFIER CIR.

703: MICROCOMPUTER INTERNAL READING CONTROL CIR.

704: READING DECODER

707: PERIPHERAL CIRCUITS

708: CONTROL BUS

710: OUTWARD READING CONTROL CIR.

711: OUT-OF-MICROCOMPUTER OUTPUT CIR.

713: MEMORY DATA OUTPUT TERMINAL

720: MICROCOMPUTER (FIRST DEVICE) NOT HAVING OUT-OF-DEVICE MEMORY DATA READING FUNCTION

725: CONTROL TERMINAL OF FIRST DEVICE

726: OUTWARD READING CONTROL TERMINAL

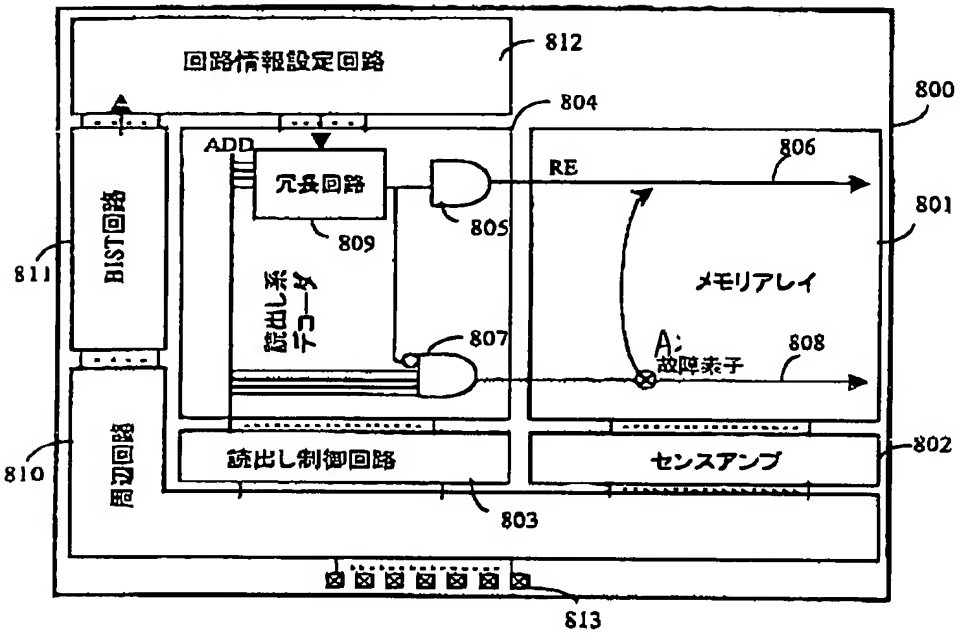
740: OUT-OF-FIRST-DEVICE READING CONTROL DEVICE (SECOND DEVICE)

742: OUTWARD READING CONTROL TERMINAL

743: OUT-OF-FIRST-DEVICE READING PERMISSION KEY INFORMATION

760: OUTWARD READING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF OUT-OF-DEVICE READING)

Fig.25



A: FAULTY ELEMENT

800: CIRCUIT IN WHICH CIRCUIT INFORMATION CAN BE SET ON THE BASIS OF BIST (BUILT-IN SELF-TEST) RESULTS

801: MEMORY ARRAY

802: SENSE AMPLIFIER CIR.

803: READING CONTROL CIR.

804: READING DECODER

805: REDUNDANT DECODER

806: REDUNDANT WORD LINE

807: DECODER

808: WORD LINE

809: REDUNDANT CIR.

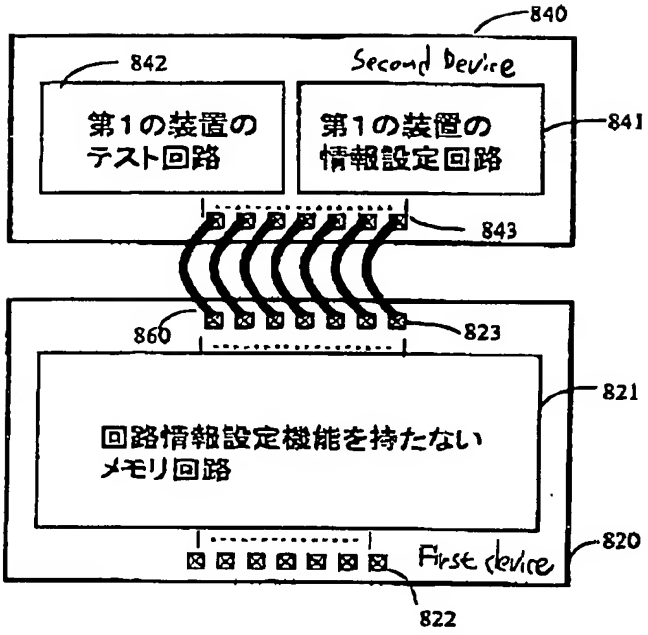
810: PERIPHERAL CIRCUITS

811: BIST (BUILT-IN SELF-TEST) CIR.

812: CIRCUIT INFORMATION SETTING CIR.

813: SEMICONDUCTOR DEVICE CONTROL TERMINAL

Fig.26



820: DEVICE NOT HAVING CIRCUIT INFORMATION SETTING FUNCTION (FIRST DEVICE)

821: CIRCUIT WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRICAL INFORMATION

822: CONTROL TERMINAL OF FIRST DEVICE

823: CIRCUIT INFORMATION SETTING TERMINAL

840: TESTING AND INFORMATION SETTING DEVICE (SECOND DEVICE) FOR FIRST DEVICE

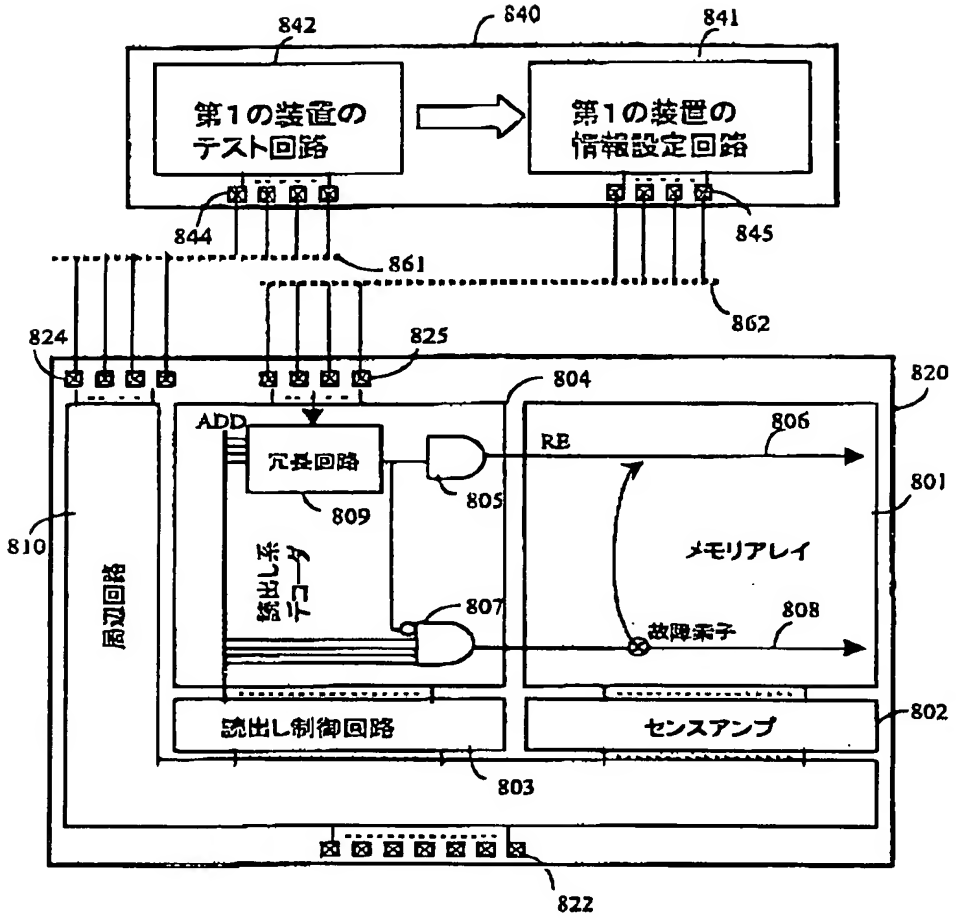
841: INFORMATION SETTING CIR. FOR FIRST DEVICE

842: TESTING CIR. FOR FIRST DEVICE

843: CIRCUIT INFORMATION SETTING TERMINAL

860: INFORMATION SETTING SIGNAL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF INFORMATION SETTING)

Fig.27



801: MEMORY ARRAY
802: SENSE AMPLIFIER CIR.
803: READING CONTROL CIR.
804: READING DECODER
805: REDUNDANT DECODER
806: REDUNDANT WORD LINE
807: DECODER
808: WORD LINE
809: REDUNDANT CIR.
810: PERIPHERAL CIRCUITS

820: DEVICE NOT HAVING CIRCUIT INFORMATION SETTING FUNCTION (FIRST DEVICE)
822: CONTROL TERMINAL OF FIRST DEVICE
824: TESTING AND CIRCUIT INFORMATION SETTING CONTROL TERMINAL
825: CIRCUIT INFORMATION SETTING TERMINAL
840: TESTING AND INFORMATION SETTING DEVICE (SECOND DEVICE) FOR FIRST DEVICE
841: INFORMATION SETTING CIR. FOR FIRST DEVICE
842: TESTING CIR. FOR FIRST DEVICE
844: TESTING AND CIRCUIT INFORMATION SETTING CONTROL TERMINAL
845: CIRCUIT INFORMATION SETTING TERMINAL
861: INFORMATION SETTING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF INFORMATION SETTING)
862: INFORMATION SETTING SIGNAL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF INFORMATION SETTING)